CLAIMS

We claim:

1. A content addressable memory (CAM) of a communications system utilizing ternary hierarchical addressing and associated address masks, said CAM comprising a plurality of address entries and associated address masks that are arranged in said CAM by mask number, with address entries having the highest mask number being located at address entry locations at the top of the CAM and address entries having the lowest mask number being located at address entry locations at the bottom of the CAM, said mask number being defined as the number of contiguous ones in an associated address mask.

2. The CAM of Claim 1 wherein said CAM is a ternary CAM.

3. The CAM of Claim 1 wherein said CAM is a binary CAM.

4. The CAM of Claim 3 further comprising binary-encoding ternary (BET) conversion means for converting each ternary value in said ternary hierarchical address into a corresponding BET value to form said address entries, said each ternary value being represented by first and second bits of said corresponding BET value as follows:

$$0_{ternary} \Rightarrow 01_{binary}$$
$$1_{ternary} \Rightarrow 10_{binary}$$
$$X_{ternary} \Rightarrow 00_{binary},$$

where X is defined as a "don't care" value, and wherein said first bit is stored in a first bit location in an upper portion of said address entry location and wherein said second bit is stored in a second bit location in a lower portion of said address entry location.

5. The CAM of Claim 4 wherein said first bit location and said second bit location are separated by a predetermined number of bit locations from each other.

6. The CAM of Claim 5 wherein said predetermined number of bit locations is 32 based on 64-bit wide CAM entry size.

7. The CAM of Claim 1 wherein said communication system is a telecommunication system.

8. The CAM of Claim 1 wherein said communication system is a data communication system.

9. The CAM of Claim 1 wherein said communication system is a network system.

10. The CAM of Claim 9 wherein said network system is the Internet Protocol (IP) network.

11. The CAM of Claim 9 wherein said network comprises layer-3 switches.

12. The CAM of Claim 9 wherein said network comprises asynchronous transfer mode (ATM) switches using E.164 addressing.

13. An apparatus for storing a plurality of address entries and associated address masks in a communication system utilizing ternary hierarchical addressing and associated address masks, said apparatus comprising:

a binary CAM;

a binary-encoded ternary (BET) conversion means coupled to said binary CAM wherein said BET conversion means converts each ternary value into a corresponding BET value to form said address entries; and

wherein said plurality of address entries and associated address masks are arranged in said binary CAM by mask number, with address entries having the highest mask number being located at address entry locations at the top of the CAM and address entries having the lowest mask number being located at address entry

locations at the bottom of the CAM, said mask number being defined as the number of contiguous ones in an associated address mask.

14. The apparatus of Claim 13 wherein said BET conversion means generates a BET value comprising a first bit and a second bit for every ternary value of the ternary hierarchical address as follows:

$$0_{ternary} \Rightarrow 01_{binary}$$
$$1_{ternary} \Rightarrow 10_{binary}$$
$$X_{ternary} \Rightarrow 00_{binary},$$

where X is defined as a "don't care" value, and wherein said first bit is stored in a first bit location in an upper portion of said CAM address entry location and wherein said second bit is stored in a second bit location in a lower portion of said CAM address entry location.

15. The apparatus of Claim 14 wherein said first bit location and said second bit location are separated by a predetermined number of bit locations from each other.

16. The apparatus of Claim 15 wherein said predetermined number of bit locations is 32 based on 64-bit wide CAM entry size.

17. The apparatus of Claim 16 wherein said communication system is a telecommunication system.

18. The apparatus of Claim 16 wherein said communication system is a data communication system.

19. The apparatus of Claim 16 wherein said communication system is a network system.

20. The apparatus of Claim 19 wherein said network system is the Internet Protocol (IP) network.

21. The apparatus of Claim 19 wherein said network comprises layer-3 switches.

22. The apparatus of Claim 19 wherein said network comprises asynchronous transfer mode (ATM) switches using E.164 addressing.

23. A method for accelerating the routing of hierarchical addressing in a communication system which utilizes ternary hierarchical addressing and associated address masks, said method comprising the steps of:

(a) obtaining communication system hierarchical addresses and associated masks to form address entries; and

(b) storing said address entries in a content-addressable memory (CAM) by mask number wherein said mask number is defined as the number of contiguous ones in an associated address mask and wherein address entries having the highest mask number are stored in address entry locations at the top of the CAM and address entries having the lowest mask number being stored at address entry locations at the bottom of the CAM..

24. The method of Claim 23 wherein said step of obtaining communication system hierarchical addresses and associated masks comprises converting the ternary hierarchical addresses and associated address masks into binary-encoded ternary (BET) to form said address entries and wherein said CAM is a binary CAM.

25. The method of Claim 24 wherein each ternary hierarchical address and associated mask comprises a plurality of ternary values and wherein said step of converting the ternary hierarchical addresses and associated address masks into BET comprises the conversion of each of the ternary values into first and second binary-encoded ternary (BET) bits as follows:

$$0_{ternary} \Rightarrow 01_{binary}$$

$$1_{ternary} \Rightarrow 10_{binary}$$
$$X_{ternary} \Rightarrow 00_{binary},$$

where X is defined as a "don't care" value.

26. The method of Claim 25 wherein said step of storing said address entries in said binary CAM comprises storing said first bit in a first bit location in an upper location of said address entry location and wherein said second bit is stored in a second bit location in a lower portion of said address entry location.

27. The method of Claim 26 wherein said first bit location and said second bit location are separated by a predetermined number of bit locations from each other.

28. The method of Claim 27 wherein said predetermined number of bit locations is 32 based on 64-wide CAM entry size.

29. The method of Claim 24 wherein said step of storing said address entries in said binary CAM comprises the following steps:

(a) logically ANDing the hierarchical address with its associated mask to form a first portion of said address entry;

(b) logically ANDing the one's complement of the hierarchical address with its associated mask to form a second portion of said address entry;

(c) selecting a CAM address entry location based on said mask number of said associated mask; and

(d) storing said first portion in an upper portion of said selected address entry location and storing said second portion in a lower portion of said selected address entry location.

30. The method of Claim 29 comprising a searching method for searching the CAM upon receipt of a particular ternary hierarchical address and associated mask input received from the communication system, said method comprising the steps of:

(a) converting the particular ternary hierarchical address input and associated mask into a BET input;

(b) storing said BET input in the upper portion of a CAM comparand register and storing the one's complement of said BET input in the lower portion of said CAM comparand register;

(c) storing said BET input in the upper portion of a CAM mask register and storing the one's complement of said BET input in the lower portion of said CAM comparand register; and

(d) forming a one-to-one correspondence of each bit stored in said CAM comparand register with a corresponding bit in said CAM address entry location and with a corresponding bit in said CAM mask register.

31. The method of Claim 30 further comprising the steps of:

(a) declaring a match between said CAM comparand register bit and its corresponding CAM address entry location bit:

(1) whenever said corresponding CAM mask register bit is a 1; or

(2) whenever said corresponding CAM mask register bit is a 0 and said corresponding CAM comparand register bit is identical to its corresponding CAM address entry location bit; and

(b) declaring no match between said CAM comparand register bit and its corresponding CAM address entry location bit whenever said corresponding CAM

mask register bit is a 0 and said corresponding CAM comparand register bit is different from its corresponding CAM address entry location bit.

32. The method of Claim 23 wherein said communication system is a telecommunication system.

33. The method of Claim 23 wherein said communication system is a data communication system.

34. The apparatus of Claim 23 wherein said communication system is a network system.

35. The apparatus of Claim 34 wherein said network system is the Internet Protocol (IP) network.

36. The apparatus of Claim 34 wherein said network comprises layer-3 switches.

37. The apparatus of Claim 34 wherein said network comprises asynchronous transfer mode (ATM) switches using E.164 addressing.

38. A method for maintaining a sorted CAM to enable longest matches in a single search cycle when hierarchical addresses are added to, or deleted from, the CAM in a communication system utilizing hierarchical addresses and associated address masks, said method comprising the steps of :

(a) segmenting the CAM into blocks wherein each block corresponds to a single hierarchical mask and wherein said blocks are arranged in the CAM such that the highest hierarchical masks are located at the lowest CAM addresses and the lowest hierarchical masks are located at the highest CAM addresses;

(b) storing hierarchical addresses according to said block having a corresponding hierarchical mask; and

(c) tracking

(1) the first address of each of said blocks (floor);

(2) the next free address of each of said blocks (nxtfree); and

(3) the size of each of said blocks.

39. The method of Claim 38 wherein if a block is full when an entry is trying to be made into said full block, said method further comprises the step of locating the closest block having at least one free memory space, thereby defining a non-full block.

40. The method of Claim 39 wherein said non-full block is located at higher CAM addresses, thereby defining blocks below said full block.

41. The method of Claim 40 further comprising the steps of:

(a) moving the contents of said floor of said non-full block to said nxtfree of said non-full block;

(b) for every block between said non-full block and said full block, in decreasing CAM address order, sequentially moving the contents of said floor of the upper block to said floor of the next lower block so that said floor of said block directly below said full block is empty, thereby defining an empty location;

(c) incrementing said floor of each of said blocks below said full block to the next higher CAM address and incrementing said nxtfree of each of said blocks below said full block to the next higher CAM address; and

(d) moving the entry into said empty location.

42. The method of Claim 39 wherein said non-full block is located at lower CAM addresses, thereby defining blocks above said full block.

43. The method of Claim 42 further comprising the steps of:

(a) moving the contents of the CAM address location that is directly above said nxtfree of the block directly below said non-full block to the CAM address location that is directly above said floor of said block that is directly below said non-full block;

(b) for every block between said non-full block and said full block, in increasing CAM address order, sequentially moving the contents of the CAM address location that is directly above said nxtfree of the directly lower block and move said contents into the CAM address location directly above said floor of said lower block so that CAM address location directly above said floor of said full block is empty, thereby defining an empty location;

(c) decrementing said floor of each of said blocks above said full block to the next lower CAM address and decrementing said nxtfree of each of said blocks above said full block to the next lower CAM address; and

(d) moving the entry into said empty location which is defined as a new floor for said full block.

44. The method of Claim 39 further comprising the step of deleting an entry from said CAM, said deleting step comprising:

(a) moving a last entry in a block into the CAM address location of said entry to be deleted; and

(b) decrementing said nxtfree of said block to CAM address location of said last entry.

45. The method of Claim 43 further comprising the step of deleting an entry from said CAM, said deleting step comprising:

(a) moving a last entry in a block into the CAM address location of said entry to be deleted; and

(b) decrementing said nxtfree of said block to CAM address location of said last entry.

46. The method of Claim 38 further including the step of searching the CAM for a single hierarchical network address entry having a mask, said single address entry searching comprising the steps of:

(a) logically ANDing the network address and its respective mask to form a first CAM entry portion;

(b) logically ANDing the one's complement of the network address and its respective mask to form a second CAM entry portion;

(c) loading said first and second CAM entry portions into a first register of said CAM; and

(d) comparing said first and second CAM entry portions with said stored hierarchical addresses.

47. The method of Claim 38 wherein said step of storing hierarchical addresses according to said block having a corresponding hierarchical mask comprises the insertion of each hierarchical address in said block in a non-sequential order.

48. The method of Claim 44 further comprising the step of interleaving steps of said maintaining a sorted CAM between steps of a searching method of said CAM in order to

maintain said sorted CAM with minimal loss in performance whenever said communication system is operating at full bandwidth.

49. The method of Claim 45 further comprising the step of interleaving steps of said maintaining a sorted CAM between steps of a searching method of said CAM in order to maintain said sorted CAM with minimal loss in performance whenever said communication system is operating at full bandwidth.

50. The method of Claim 38 wherein said communication system is a telecommunication system.

51. The method of Claim 38 wherein said communication system is a data communication system.

52. The method of Claim 38 wherein said communication system is a network system.

53. The method of Claim 52 wherein said network system is the Internet Protocol (IP) network.

54. The method of Claim 52 wherein said network comprises layer-3 switches.

55. The method of Claim 52 wherein said network comprises asynchronous transfer mode (ATM) switches using E.164 addressing.